

# A 2.5 V CMOS DIFFERENTIAL ACTIVE INDUCTOR WITH TUNABLE L AND Q FOR FREQUENCIES UP TO 5 GHZ

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**Abstract** — A differential active inductor in CMOS-technology with a supply voltage of 2.5 V is presented. A self-resonant frequency of 5.6 GHz is achieved. The value of the inductance  $L$  can be controlled in the range from 10 nH up to 100 nH. The quality factor  $Q$  can be tuned independently of  $L$  to values as large as 600. The active inductor is realized with a differential gyrator. The gyrator transforms intrinsic capacitances of the MOSFETs to the emulated inductance.

## I. INTRODUCTION

With decreasing channel length and therefore increasing transit frequency CMOS technology becomes an attractive candidate for integrated RF circuits. Inductors are key elements for filtering and matching in RF circuits. But on-chip spiral inductors exhibit poor quality factors and require large die area. Therefore active inductors are attractive to save die area and to realize circuits like filters, tuned amplifiers and oscillators.

The active inductor presented here provides independent tuning of the inductance value  $L$  and the quality factor  $Q$ . The tuning is performed without using varactors. This tuning feature can ease the design of amplifiers and oscillators with tuned maximum gain or oscillation frequency.

## II. CIRCUIT DESIGN AND ANALYSIS

### A. Circuit Design

A simplified schematic of the circuit is given in Fig. 1. A gyrator is realized by connecting two differential transconductance amplifiers back to back. A negative resistance load is connected at the output of both differential stages to control the output conductance of the transconductance amplifiers. The current sources ( $I_L$ ,  $I_{Q1}$ ,  $I_{Q2}$ ) are realized by NMOS- and PMOS-current mirrors that are controlled by 3 external currents ( $I_{L\text{ref}}$ ,  $I_{Q1\text{ref}}$ ,  $I_{Q2\text{ref}}$ ) applied to the circuit.

The circuit schematic with bias network is given in Figure 2. In comparison to the active inductor presented in [1], our circuit uses a circuit topology that reduces the current consumption in the negative resistance loads. This

is realized by using PMOS current sources instead of PMOS load transistors. Transistors used as current sources provide a lower output conductivity than load transistors, therefore the negative resistance transistors can be designed with less gate width and consume less current. The PMOS- and NMOS-current sources are controlled simultaneously by the external currents. The control of the PMOS current-sources is realized with PMOS-current mirrors adding the currents  $I_{L\text{ref}}$  and  $I_{Q1\text{ref}}$  or  $I_{Q2\text{ref}}$ , respectively. Additional on-chip capacitors and resistors provide on-chip filtering of the bias currents and the supply voltage to prevent disturbances while measuring the circuit.

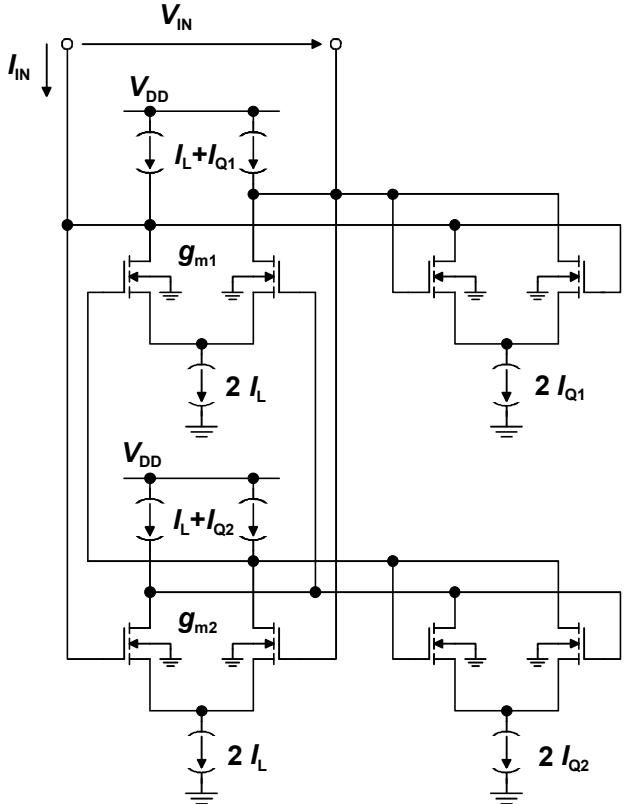


Fig. 1. Principal schematic of the active inductor

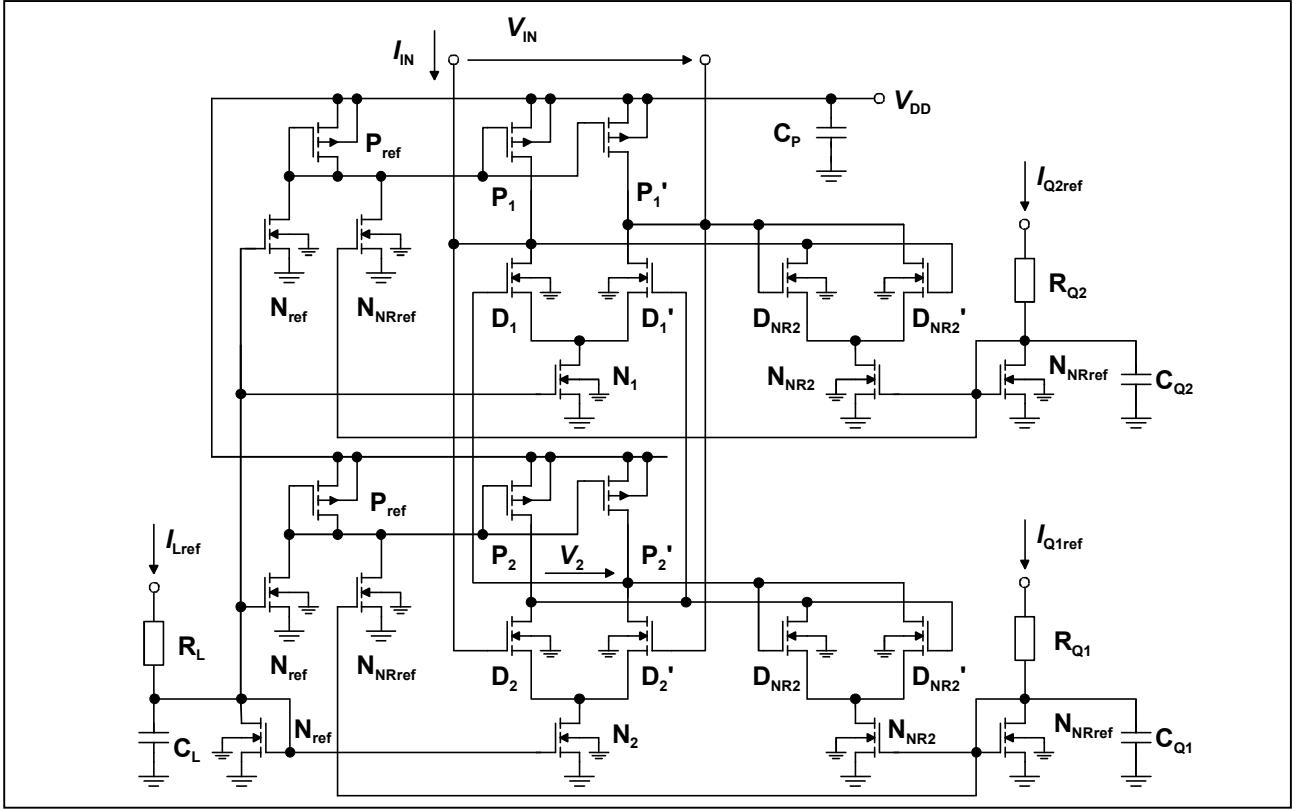


Fig. 2. Schematic of the active inductor with bias circuitry

### B. Circuit Analysis

To calculate the input impedance of the circuit, all MOSFETs connected to the signal nodes are modeled by an equivalent circuit comprising the transconductance  $g_m$ , the output conductivity  $g_d$  and the capacitors  $C_{gs}$ ,  $C_{gd}$  and  $C_{db}$ .  $C_{db}$  has to be taken into account, because it is almost as large as  $C_{gs}$  for the short channel devices used in our design. The source node of each MOSFET is on RF virtual ground, therefore  $C_{sb}$  can be omitted.

The circuit can be divided into two symmetrical half-circuits. Figure 3 shows the small-signal, differential-mode equivalent circuit of the half-circuit.

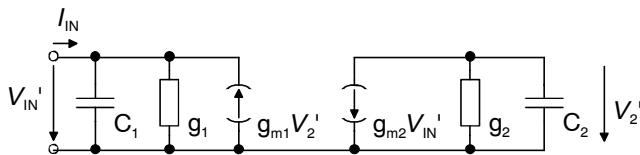


Fig. 3. Small-signal, differential-mode equivalent circuit of half the active inductor

$C_{1(2)}$  is the total effective capacitance between one of the drain nodes of the transconductance amplifier stage 1 (2) and ground. The conductance  $g_{1(2)}$  is the effective output conductance at the drain node, the value of the negative conductance taken into account. Finally  $g_{m1(2)}$  is the transconductance of the differential pair transistors in stage 1(2). The feedforward paths through  $C_{gd}$  of the differential pairs compensate for each other, when both differential pairs have the same size. With the equivalent circuit of figure 3, the differential mode input impedance is calculated as follows:

$$Z_{IN} = 2 \frac{V_{IN}'}{I_{IN}} = 2 \frac{g_2 + sC_2}{[g_{m1}g_{m2} + g_1g_2] + s[g_1C_2 + g_2C_1] + s^2C_1C_2} \quad (1)$$

The transconductances  $g_{m1}$  and  $g_{m2}$  are tuned simultaneously by the current  $I_{Lref}$ . The output conductances  $g_1$  and  $g_2$  are tuned by adjusting the currents  $I_{Q1ref}$  and  $I_{Q2ref}$ .

A simplified equivalent circuit of the active inductor in differential mode is given in Figure 3. The elements  $L$ ,  $R$ ,  $G$  and  $C$  are given in equation (2).

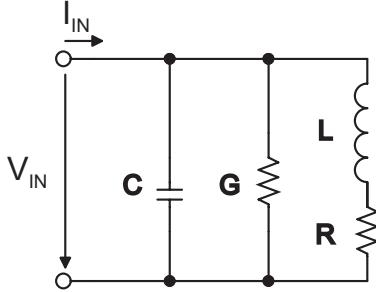


Fig.4 Simplified equivalent circuit of the active inductor

$$\begin{aligned} L &= \frac{2C_2}{g_{m1}g_{m2}} \\ R &= \frac{2g_2}{g_{m1}g_{m2}} \\ G &= \frac{1}{2}g_1 \\ C &= \frac{1}{2}C_1 \end{aligned} \quad (2)$$

The inductance  $L$  is tuned via  $g_{m1}$  and  $g_{m2}$  (which are corresponding to the current  $I_{L\text{ref}}$ ). The quality factor  $Q$  is tuned by adjusting  $R$  and  $G$  via  $g_1$  and  $g_2$  (which are corresponding to the currents  $I_{Q1\text{ref}}$  and  $I_{Q2\text{ref}}$  respectively).

The long-channel approximation is valid for the MOSFETs in the chosen operating point, therefore the inductance  $L$  has the following dependency on the bias current  $I_{L\text{ref}}$ :

$$L \sim \frac{1}{g_{m1}g_{m2}} \sim \frac{1}{\sqrt{I_{L1}I_{L2}}} \sim \frac{1}{I_{L\text{ref}}} \quad (3)$$

A tuning range of 1:10 can be achieved.

#### IV. LAYOUT

The active inductor was designed for a  $0.3 \mu\text{m}$  CMOS process with a transit frequency of  $f_T = 40 \text{ GHz}$ . The process offers three metal layers on high resistive substrate. The circuitry of the inductor itself without pads and additional capacitors occupies an area of about  $200 \mu\text{m} \times 200 \mu\text{m}$ . To test the circuit, the RF signal of an network analyzer is balanced with a  $180^\circ$ -hybrid and applied to the circuit with two GSG-probes.

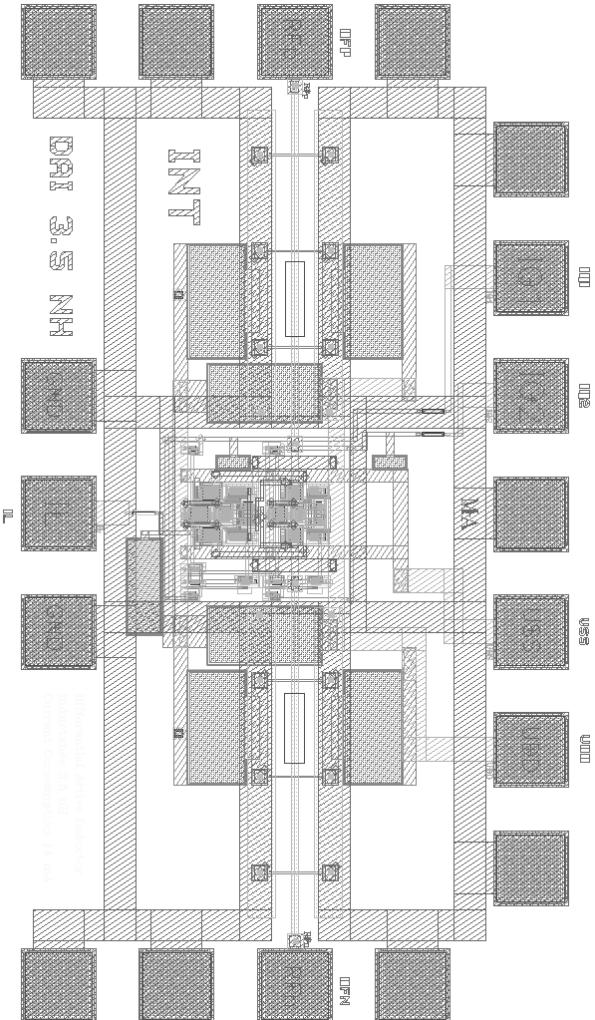


Fig. 5 Layout of the active inductor

#### V. SIMULATION RESULTS

To get an inductance of  $10 \text{ nH}$ ,  $I_{L\text{ref}}$  is set to  $1.0 \text{ mA}$ ,  $I_{Q1\text{ref}}$  and  $I_{Q2\text{ref}}$  are set to  $126 \mu\text{A}$  and  $123 \mu\text{A}$  respectively. With this bias, the circuit consumes  $6 \text{ mA}$  from a  $2.5 \text{ V}$  supply. The simulated impedance magnitude, phase and quality factor are shown in figure 6. The self resonant frequency of the active inductor is  $5.6 \text{ GHz}$ . The quality factor is larger than  $100$  in from  $400 \text{ MHz}$  to  $4 \text{ GHz}$  and reaches  $600$  at  $2 \text{ GHz}$ . If the currents are reduced to  $I_{L\text{ref}} = 100 \mu\text{A}$ ,  $I_{Q1\text{ref}} = 13.5 \mu\text{A}$  and  $I_{Q2\text{ref}} = 11.6 \mu\text{A}$ , an inductance value of  $100 \text{ nH}$  is achieved with a DC-current consumption of  $850 \mu\text{A}$ . The self resonant frequency decreases to  $1.8 \text{ GHz}$ . This results in a frequency band with a  $Q$  value larger than  $100$  between  $100 \text{ MHz}$  and  $1 \text{ GHz}$  with the maximum  $Q$  of  $350$  at  $450 \text{ MHz}$  (see figure 7).

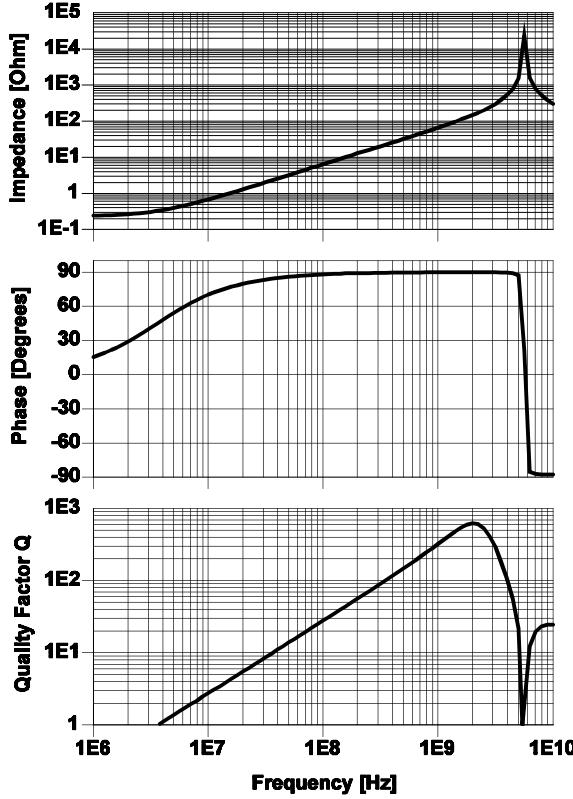


Fig. 6 Simulation results with bias for 10 nH

Due to the drain current noise of the MOSFET, the active inductor exhibits relatively poor noise performance. The input referred noise current density (equivalent noise current source in parallel to the input port) is 25 pA/ $\sqrt{\text{Hz}}$  at 2 GHz for the 10 nH bias. The noise current is independent of the chosen quality factor.

Due to the fully differential and balanced architecture of the circuit, the large signal performance of the circuit is acceptable. With an applied input voltage swing of 80 mV at 1.2 GHz, a input current swing of 1.0 mA with a THD of 1.3 % can be achieved for the 10 nH bias, which corresponds to an AC current amplitude through a  $g_{m1}$  differential pair transistor ( $\bar{I} = 0.5$  mA) of about 50 % the DC value ( $I_L = 1.0$  mA). If the frequency is increased to 4 GHz, an input voltage swing of 250 mV can be applied, resulting in an input current swing of 450  $\mu$ A with a THD of 1.5%.

## V. CONCLUSION

A CMOS differential active inductor with tunable  $L$  (10 nH to 100 nH) and tunable  $Q$  (up to 600) is designed and presently in the fabrication process. The simulated self resonant frequency is 5.6 GHz for the 10 nH-bias with a

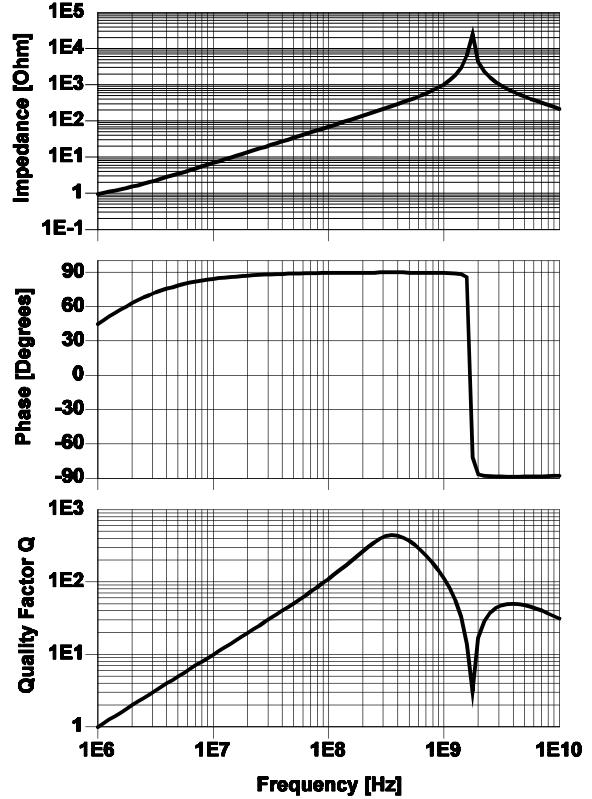


Fig. 7 Simulation results with bias for 100 nH

power consumption of 15 mW. This self resonant frequency is higher than the values reported in [1] (1 GHz) and [2] (1.7 GHz). With the bias tuned for 100 nH, the power consumption drops to 2 mW, whereas the self resonant frequency is still 1.8 GHz. The active inductor exhibits a relatively large input referred noise current but sufficient large signal performance.

## ACKNOWLEDGEMENT

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## REFERENCES

- [1] A. Thanachayanont and A. Payne, "CMOS floating active inductor and its applications to bandpass filter and oscillator designs," *IEE Proceedings – Circuits, Devices and Systems*, vol. 147, no. 1, pp. 42-48, February 2000.
- [2] R. Akbari-Dilmaghani, A. Payne and C. Toumazou, "A High Q RF CMOS Differential Active Inductor," *1998 IEEE International Conference on Electronics, Circuits and Systems*, Part vol. 3, pp. 157-160, 1998.